IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
Chuan-Jen Wu	§	Group Art Unit: Unknown
	§	
Serial No. Unknown	§	
	§	Examiner: Unknown
Filed: Herewith	§	
	§	
For: Job Flow Petri Net and Controlling Mechanism For Parallel Processing	§	

INFORMATION DISCLOSURE STATEMENT

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

The above-identified application is being after June 30, 2003. Therefore, pursuant to the waiver of the requirement under 37 CFR 1.98 (a)(2)(i) as stated in a Pre-OG Notice dated July 11, 2003, copies of only the foreign patent documents and non-patent literature listed on the enclosed modified Form PTO-1449 are attached.

This Information Disclosure Statement is being filed within three months of the United States filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required (37 CFR §1.97(b)).

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

David M. O'Dell
Registration No. 42,044

Date: 4-14-04

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R-72254.1

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 4-14-04.

Bonnie Boyle
Printed Name

Bonnie Boyle
Signature

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	
				Filing Date	Herewith
				Applicant(s)	Chuan-Jen Wu
				Art Unit	
				Examiner Name	
SHEET	1	OF	2	Attorney Docket Number	24061.48 (TSMC2003-0059)

U. S. PATENT DOCUMENTS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	AA	5,050,088	09-17-1991	Buckler et al.
	AB	5,121,003	06-09-1992	Williams
	AC	5,283,896	02-01-1994	Temmyo et al.
	AD	5,513,132	04-30-1996	Williams
	AE	5,555,179	09-10-1996	Koyama et al.
	AF	5,671,151	09-23-1997	Williams
	AG	6,286,033	09-04-2001	Kishinsky et al.
	AH	6,314,553	11-06-2001	Stevens et al.
	AI	6,349,238	02-19-2002	Gabbita et al.
	AJ	6,421,808	07-16-2002	McGeer et al.
	AK	2003/0018512	01-23-2003	Dortmans

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	AL	JP – 07-56886	03-03-1995	Noriaki et al.	N

OTHER PRIOR ART		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AM	HYUN JOONG YOON et al., "Identification of Potential Deadlock Set in Semiconductor Track Systems", Proceedings of the 2001 IEEE Int'l Conference on Robotics & Automation, May 21-26, 2001, pgs. 1820-1825, Seoul, Korea
	AN	JIN YOUNG CHOI et al., "A Generalized Stochastic Petri net Model for Performance Analysis and Control of Capacited Re-entrant Lines", IEEE Transactions on R&A, 2003, 9 pgs., Volume XX.
	AO	ROBERT ESSER, et al., "Applying an Object-Oriented Petri Net Language to Heterogeneous Systems Design", 9 pgs.
	AP	MARK LaPEDUS, "Is e-diagnostics dead or alive in the industry?", Silicon Strategies, July 15, 2003, 3 pgs., Semiconductor Business News
	AQ	MU DER JENG et al., "Modeling, Qualitative Analysis, and Performance Evaluation of the Etching Area in an IC Wafer Fabrication System Using Petri Nets, IEEE Transaction on Semiconductor Manufacturing, Vol II, No. 3, 16 pgs., August, 1998.

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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				Filing Date	Herewith
				Applicant(s)	Chuan-Jen Wu
				Art Unit	
				Examiner Name	
SHEET	2	OF	2	Attorney Docket Number	24061.48 (TSMC2003-0059)

U. S. PATENT DOCUMENTS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document

FOREIGN PATENT DOCUMENTS					
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OTHER PRIOR ART		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AR	R. S. SRINIVASAN, "Modeling and Performance Analysis of Cluster Tools Using Petri Nets, IEEE Transactions on Semiconductor Manufacturing, Vol. II, No. 3, 10 pgs., August 1998
	AS	MENGCHU ZHOU et al., "Modeling, Analysis, Simulation, Scheduling, and Control of Semiconductor Manufacturing Systems: A Petri Net Approach", IEEE Transactions of Semiconductor Manufacturing, Vol. II, No. 3, 25 pgs., August 1998.

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.